A-level Computer Science

Types of processor

Lesson Objectives

Students will learn about:

- Issues in von Neumann architecture
- Difference between von Neumann and Harvard architectures
- CISC and RISC processor types
- Co-processor systems
- Parallel processor systems

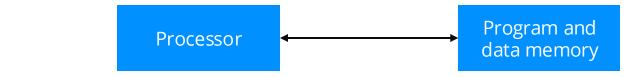


Content

Issues in von Neumann architecture



- Data and programs share the same memory.
- A program may overwrite data with programming instructions if not written carefully.
- Also, programming instructions may also be overwritten with data.
- The programming instructions and data share the same bus. This makes the processor slow as it waits for instructions.



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Issues in von Neumann architecture

- Instructions and data share a single address bus.
- The word size used for both instructions and data is the same.

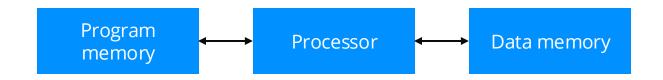
Address	Contents	
1000	Instruction	
1001	Instruction	
1002	Instruction	
1003	Instruction	
•••	•••	
100A	Data	
100B	Data	



Harvard architecture



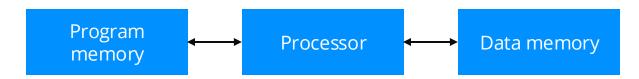
- The issues in the von Neumann architecture are overcome in Harvard architecture.
- Harvard architecture uses two separate memory spaces for program and data.
- This also ensures that there are two separate buses.



Harvard architecture



- The processor is now able to process both program and data simultaneously.
- This improves the processing speed.
- The chances of data being overwritten by programming instructions or vice versa are now nullified.



Harvard architecture



- The characteristics of program memory and data memory may be different.
- For example: Program memory shall be a read-only memory whereas data memory shall be a read-write memory.

		von Neumann architecture	Harvard architecture
	Application	PCs, servers and simple embedded	Digital signal processing, image
		systems	processing, audio processing in embedded systems
nn	Sharing in	Programs and data	Program and data are
ard	memory unit	share the same memory unit	stored in separate memory units
cture	Bus	Single bus for	Program and data have
		transferring data and	different buses that
		instructions	can be used
			simultaneously
	Program	Optimised programs	Programs with larger
		are used	memory requirements
			can be used

von Neumann vs Harvard architecture

Computer architecture



- In modern computers, both Harvard and von Neumann architectures are used.
- The main memory follows the von Neumann architecture.
- Whereas, the cache memory follows the Harvard architecture and has instruction cache and data cache.
- Advanced digital signal processors provide multiple buses for data transmission with separate buses for read and write operations.

Processor type

The two main types of computer processors are:

- Complex Instruction Set Computing (CISC)
- Reduced Instruction Set Computing (RISC)



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	Complex Instruction Set Computing (CISC)	Reduced Instruction Set Computing (RISC)
Architecture	By Intel or AMD	ARM architecture
Instructions	Hundreds of instructions	RISC has fewer instructions when compared to CISC. To perform complex functions, simple tasks are combined.
Instruction cycle	Complex instruction cycle	Simple instruction cycle and, hence, is more efficient at simpler tasks
Physical size	Larger CPUs and memory to handle the large number of instructions	Smaller when compared to CISC

	Complex Instruction Set Computing (CISC)	Reduced Instruction Set Computing (RISC)
Speed	Higher clock speed. Best suited for intensive tasks	Lower clock speed. Performs simpler tasks faster
Energy consumption	Larger CPUs needs more power	Designed for less power consumption
Design	Usually built on a system with cooling fan and heat sink	Memory and other hardware are combined with CPU on a single chip
Cost	Expensive than RISC	Less expensive
Examples	Desktop and laptop computers	Smart phones and tablets

	CISC processor (8086) (Division)	RISC processor (8085) (Repeated subtraction)	
	MOV AX, 3F4E	3000	LXI H, 1040
	MOV BX, 4E	3003	MOV B, M
	DIV BX	3004	MVI C, 00
Programs for		3006	INX H
dividing two		3007	MOV A, M
0		3008	CMP B
numbers in		3009	JC 3011
CISC and RISC		300C	SUB B
processors		300D	INR C
p10000010		300E	JMP 3008
		3011	STA 2040
		3014	MOV A, C
		3015	STA 2041
		3018	HLT
	Divides the number in register	Loads the register A and B with numbers in	
	AX by number in register BX and	memory location 1040 and 1041 respectively.	
	stores the result in register A	Repeated subtraction is performed to divide	
	(Quotient in AL and remainder in	the two numbers. Stores the quotient in 2041	
	AH).	and remainder in 2040.	

CISC vs RISC programming

CISC

Uses a single line instruction to divide two numbers. The processor is capable of understanding and performing the sub-tasks involved to divide two numbers.

Compiler's operation of translating a code in a high-level language to machine code is simple.

Too many instructions in a CISC processor is a disadvantage because it occupies memory, and some advanced instructions are not used often.

RISC

Does not have an in-built DIV instruction and uses the repeated subtraction technique to divide two numbers. This also increases the execution time.

The compiler's operation is slightly complicated.



Co-processor systems

- The co-processor is an additional processor that performs certain supplementary functions of the primary processor.
- Responsible for a limited range of functions such as digital signal processing, floating-point arithmetic and others.

Graphics Processing Unit (GPU)

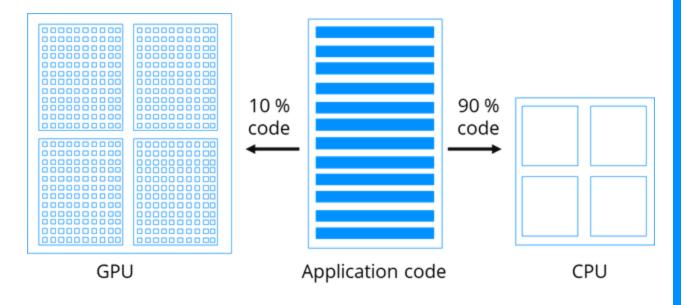


- GPU is a co-processor, made of a specialized electronic circuit that accelerates computer analysis by offloading computerintensive instructions while the remaining instructions run on the processor.
- GPU is used for manipulating images and graphics.
- The presence of GPU enhances the performance of the computer.

GPU

A CPU consists of few cores well suited for sequential serial processing.

Whereas, a GPU consists of several smaller but efficient cores for huge parallel processing.





Parallel processor systems

- When executing instructions, the instructions from the main memory flows to the processor and the operands flows to and from the processor.
- The instruction and data streams in a simple computer are given in figure.
 Processor (P)
 Memory (M)

Data stream



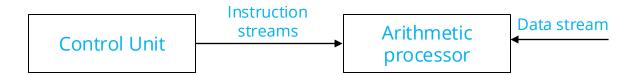
Parallel processor systems

- There are four different types of processor systems:
- SISD (Single Instruction Single Data Stream)
- SIMD (Single Instruction Multiple Data Stream)
- MISD (Multiple Instruction Single Data Stream)
- MIMD (Multiple Instruction Multiple Data Stream)



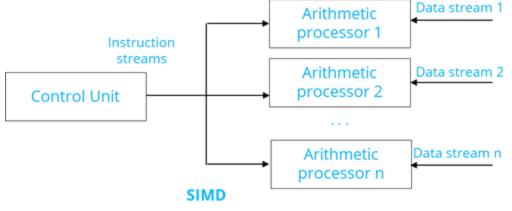
SISD (Single Instruction Single Data Stream)

- In this processor system, there is a single processor.
- Instructions are executed sequentially but pipelining of instructions may occur.
- Different function units are possible, but all the units are controlled by a single control unit. Example: Intel Pentium 4



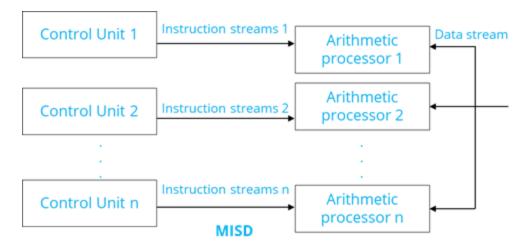
SISD (Single Instruction Multiple Data Stream)

- In a SIMD processor system, there is an array of processors.
- Each processor has its own memory and receives the same instruction.
- When executing instructions, each processors uses its own dedicated memory. All the processors are controlled by a single control unit.



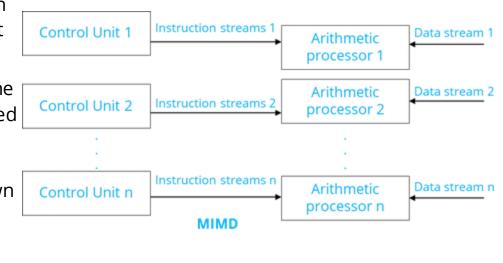
MISD (Multiple Instruction Single Data Stream)

- In this system, there are several processor units and each processor unit has its own control unit.
- This is not used in commercial products.



MISD (Multiple Instruction Multiple Data Stream)

- In MIMD systems, there are multiple processors, and each processor receives a different instruction.
- Data stream is provided by the memory unit and is partitioned based on the number of processor units. Each processor unit also has its own cache memory. Personal computers follow this system of processors.



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Let's review some concepts

von Neumann Vs. Harvard

von Neumann: Same memory space for program and data memory.

Harvard: Separate memory spaces for program and data memory.

CISC vs. RISC

CISC: Hundreds of instructions

RISC: Fewer instructions compared to CISC.

Application

von Neumann: main memory

Harvard: cache

Co-processor

An additional processor that performs certain supplementary functions of the primary processor.

Graphics Processing Unit (GPU)

A co-processor, made of a specialised electronic circuit that accelerates computer analysis by offloading computer-intensive instructions while the remaining instructions run on the processor.

Processor types

The two main types of computer processors are: Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC).

Parallel processor systems

SISD (Single Instruction Single Data Stream) SIMD (Single Instruction Multiple Data Stream) MISD (Multiple Instruction Single Data Stream) MIMD (Multiple Instruction Multiple Data Stream) 25



Activities

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Activity-1 (Internet Research) Duration: 10 minutes

AVR microcontrollers use modified Harvard architecture. Use the internet to learn about this type of architecture and answer the following questions.

- 1. List some of the features of modified Harvard architecture.
- 2. Compare modified Harvard architecture with von Neumann architecture. List the similarities and differences.
- 3. Compare modified Harvard architecture with Harvard architecture. List the similarities and differences.

Activity-2 (Internet Research) Duration: 20 minutes	Memory location	Instruction
	3000	LXI H, 1040
1. In this topic, code for the division of	3003	MOV B, M
two numbers in 8085 microprocessor	3004	MVI C, 00
•	3006	INX H
(RISC) was given. The instruction set	3007	MOV A, M
consists of the function of each	3008	CMP B
	3009	JC 3011
instruction.	300C	SUB B
A Drowco for the instruction set of this	300D	INR C
A. Browse for the instruction set of this	300E	JMP 3008
microprocessor and list the function	3011	STA 2040
of each instruction used in this	3014	MOV A, C
	3015	STA 2041
program.	3018	HLT

Activity-2 (Internet Research) Duration: 20 minutes	Memory location	Instruction
	3000	LXI H, 1040
	3003	MOV B, M
P. Consider that the value in memory	3004	MVI C, 00
B. Consider that the value in memory	3006	INX H
location 1040 is 7h and the value in	3007	MOV A, M
memory location 1041 is 95h. What	3008	CMP B
-	3009	JC 3011
will be the values stored in memory	300C	SUB B
location 2040 and 2041 after the	300D	INR C
	300E	JMP 3008
execution of this program?	3011	STA 2040
	3014	MOV A, C
	3015	STA 2041
	3018	HLT



End of topic questions

End of topic questions

- 1. What are the issues in von Neumann architecture?
- 2. What is Harvard architecture? How is it different from von Neumann architecture?
- 3. Compare the RISC architecture with CISC architecture.
 - a. State any 5 differences.
 - b. In what ways is RISC architecture better than CISC architecture?
 - c. The assembly language of which of the two architectures is easier for the programmer to code? Why?

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End of topic questions

- 4. What is a Graphics Processing Unit? How does it work with the CPU to run a computer intensive application code?
- 5. What are the four different processor systems? How are they different from each other?